Visible & Infrared Survey Telescope for Astronomy

IR CAMERA

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Change Record

Issue	Date	Section(s) Affected	Description of Change/Change Request Reference/Remarks
1.0	06-03-02	Not Applicable	First Issue
1.1	04-07-02	All	Updated to reflect selection of Raytheon detectors; updated block diagrams included; more detailed software specs.
1.2	16-08-02	5.15, 5.17,5.19,5.20, 5.21, 5.22, 5.25, 5.29 and appndx-3	16 detectors; window readout with detector architecture limitations, controller drift and earthquake loads redefined. Appendix-3 updated with Raytheon latest signals.
1.3	22-08-02	1, 2, 3, 4, 5.6, 5.15, 5.16, 5.17, 5.21, 5.25, 5.29 and 6	Separate section (6) (from Malcolm) has been added mentioning ESO and VPO responsibilities. Steven Beard comments (from 5th July mail) are incorporated which avoid spec duplications, and moving specs to relevant sections.
1.4	23/08/02	All	Document issued to ESO
1.5	18/02/03 to 20/02/03	All	Doc No changed to –06035-0005; reformatted using IR Camera Template. Number cruncher & networks defined more generally, Master Clock distribution, DBE functions performed in ESO PCI card. Naidu's suggestions included.
1.6	10/03/03	All	Updated after ESO/ATC/RAL teleconference
1.7	24/03/03	All	Diagrams updated, draft section 5.30 added
1.8	23/07/03 to 4/08/03	Fig.1, 5.16, 5.21, 5.30, Appendices 1 & 2	Diagrams updated, integer data vs floating point, mech/thermal interface updated. Readout status flag added. Issued to ESO for comment.

Notification List

The following people should be notified by email that a new version of this document has been issued and is available on the IR Camera Sharepoint database:

VPO:	Alistair McPherson	Danny Duff	Malcolm Stewart
RAL:	Kim Ward	Martin Caldwell	Guy Woodhouse
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1 SCOPE

This document is the technical specification defining the technical requirements for the IR Camera Detector Controller for the VISTA Telescope. The Controllers form a key part of the overall VISTA system and are required to be compatible with the standard ESO telescope control system. The IRACE (InfraRed Array Controller Electronics) Controller System produced by ESO has been selected for this purpose. The VISTA IR Camera will have a mosaic array of 16 Raytheon VIRGO IR detectors at its focal plane. In order to control these detectors, the electronic units of IRACE controller are linked in such a manner that the detectors can be read out synchronously in order to avoid interference.

In addition to the principal task summarised above, there is also a need for a reduced functionality Controller System suitable for controlling one or two IR detectors during detector evaluation and characterisation. A so-called 'Test IRACE' will be used for this purpose.

The internal architecture of the IRACE Detector Controller System, as envisaged for VISTA use, is described in this document for information purposes only. The internal architecture and design do not constitute formal requirements.

2 ACRONYMS, ABBREVIATIONS & DEFINITIONS

2.1 Acronyms and Abbreviations

ATC	Astronomy Technology Centre
DBE	Detector Back-End Electronics
DCS	Detector Control Software
DFE	Detector Front-End Electronics
DMA	Dynamic Memory Access
EMI	Electromagnetic Interference
ESO	European Southern Observatory
GIGA	High Speed Data Link
GUI	Graphical User Interface
IR	Infrared
IRACE	Infrared Array Controller Electronics
LAN	Local Area Network
MLE	Maximum Likely Earthquake
NC	Number Cruncher
OBE	Operating Basis Earthquake
ppm	parts per million
QE	Quantum efficiency
RAL	Rutherford Appleton Laboratory
rms	root mean square

ROI	Region Of Interest
RTD	Real Time Display
TBC	To Be Confirmed
TBD	To Be Decided
UT	Universal Time
VISTA	Visible and Infrared Survey Telescope for Astronomy
VPO	VISTA Project Office

2.2 Definitions

Detector Controller System: A system comprising hardware and software that can control and acquire data from one or more detectors, display these data and store them.

IRACE: An IR Detector Controller System provided by ESO. The IRACE system described in this document can operate synchronously 16 Raytheon VIRGO 2K x 2K detectors as shown in Appendix 1

Test IRACE: An IRACE system, requiring less hardware than the complete IRACE system, used to test and characterise one or two detectors. A block diagram of a Test IRACE is shown in Appendix 2.

Number Cruncher: A commercial work station that processes IRACE data in real time, sending the averaged or intermediate frames to the Instrument Work Station via a LAN.

3 APPLICABLE DOCUMENTS

[AD01] *IR Detector Controller Statement of Work,*VIS-SOW-ATC-06020-0004, Issue 1.0, 6 March 2002

[AD02] *VLT Electronics Design Specification*, VLT-SPE-ESO-10000-0015, Issue 5, 6 March 2001

[AD03] *EMC and Power Quality Specification. Part 1,* VLT-SPE-ESO-10000-0002, Issue 2, 11 March 1992

[AD04] *EMC and Power Quality Specification. Part 2*, VLT-SPE-ESO-10000-0003, Issue 1, 5 February 1992

[AD05] *VLT Instrument Software Specification*, VLT-SPE-ESO-17212-0001, Issue 2.0, 12 April 1995

[AD06] Acceptance Procedure Electrical Safety & EMC, VLT-VER-ESO-10000-0958, Issue 2, 1 March 1996

[AD07] VLT Environmental Specification, VLT-SPE-10000-0004 Issue 6, 12 November 1997

[AD08] VLT Guidelines for the Development of VLT Application Software, VLT-MAN-ESO-17210-0667, Issue 1.2, 8 October 2001

[AD09] VLT Base Instrument Control System User Manual, VLT-MAN-ESO-17240-0934, Issue 3, 31 March 2002

[AD10] Data Interface Control Document, GEN-SPE-ESO-19400-0794 Issue 1.1, 25 November 1997

[AD11] IRACE DCS User Manual, VLT-MAN-ESO-14100-1878, Issue 1.3, 20-Feb-2001.

4 THE IRACE SYSTEM

IRACE is a modular system of electronic units and associated software. As envisaged for VISTA use, the electronics comprise one or more units of: detector front-end electronics (DFE) and number crunchers (NC).

The NCs will be one or more commercial computers and it is expected that the functions normally performed by the detector back-end electronics, will be performed by GIGA-PCI cards (ESO design) in the number crunchers. The connection between DFEs and GIGA-PCI cards is via fiber optic links.

The DFEs will be located close to the cryostat and consist of a timing sequencer, clock and bias modules, acquisition modules and a high speed data link (GIGA) modules. It is expected that only 1 DFE (the Master) will produce clock & synchronisation signals. The other DFEs will be known as Slaves.

The software for IRACE includes the controller programming software, associated programming tools and the data acquisition software with a graphical user interface. Some software components run on the controller hardware and some run on the Instrument Workstation as defined in AD05.

A block diagram of the system is shown in Figure 1.

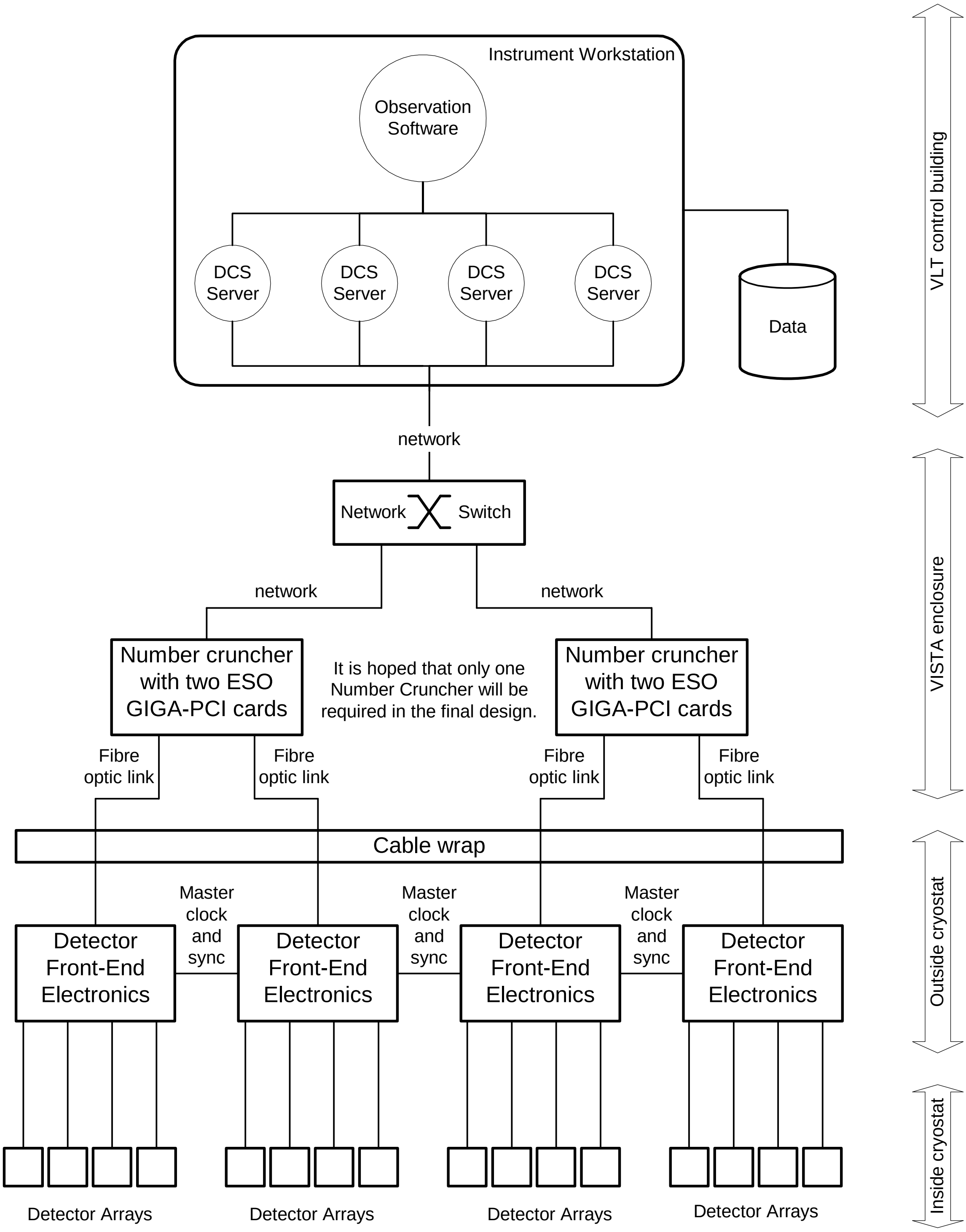


Figure 1. Block diagram showing the possible main components of the IRACE system and its externals.

5 REQUIREMENTS

5.1 Interfaces

The IRACE System shall have the following interfaces :

- Electronics interface to detectors
- LAN connections to the Instrument Workstation
- Software interface to the Observation Software running on the Instrument Workstation
- Time reference system
- Cooling
- Electrical
- Mechanical

5.2 Multiple Readout Operation

The IRACE System shall be able to operate simultaneously 16 Raytheon VIRGO detectors. A possible architecture for the distributed IRACE system for 16-detectors is given in Appendix 1.

The Test IRACE System shall be able to operate one or two 2K x 2K VIRGO detectors to allow test and characterisation of one or two detectors in the IR focal plane array. The architecture of the Test IRACE system is given in Appendix 2.

5.3 Compatibility with Raytheon VIRGO Detectors

The IRACE System shall be able to control the Raytheon VIRGO detectors, and be capable of reading all 16 video outputs from each detector simultaneously at a speed corresponding to the readout time specified in Section 5.4. The controller shall be able to supply all the necessary bias voltages, clock voltages, control signals and proper sequence of clocks as required for VIRGO devices. The details of the electrical signals for the VIRGO detector are given in Appendix 3.

In case the controller utilises distribution of Master Clock and ADC Sync pulses, the sequencer shall have sufficient drive capability to ensure that the pulses can be distributed among the IRACE DFEs, whilst maintaining sufficiently low timing jitter and pulse rise / fall times so as not to compromise the signal sampling from individual detectors. Furthermore the controller performance shall not degrade due to the distribution of conversion / sync pulses (e.g. no inherent ground loops).

5.4 Array Readout Time

The controller shall be able to read the data off the entire focal plane array in less than 1s (goal : 700ms).

5.5 Exposure Restart Time

It shall be possible to start an exposure within 5s of the completion of the previous exposure, such that the data from the previous exposure is properly stored.

5.6 Rapid Sequence of Exposures

a) It shall be possible to perform a predefined number of exposures, and store their data, such that a new exposure is started every 10s and the delay between completing one exposure and starting the next is less than 1s.
b) It shall be possible to difference and co-add exposures in situ.
c) It shall be possible to perform data acquisition and store exposures within a sequence of one raw data frame every 10s or one set of co-added data every 20s.

5.7 Exposure Accuracy

The duration of an exposure shall be within 0.1s or 1% of that requested, whichever is the larger.

5.8 Exposure Accuracy Recorded

Header data stored with the exposure shall allow the duration of an exposure at any point in the field to be determined to an accuracy of 0.01s or 0.25% whichever is the larger.

5.9 Absolute Timing

The absolute time of an exposure, readout rate and time-order of pixel readout shall be recorded such that with suitable software (not supplied) the absolute UT of mid-exposure at each pixel can be determined to within 0.1s (TBC).

5.10 Operation with Subset of Detector Arrays

As far as practicable, it shall be possible to operate the controller with any number of arrays disabled, subject to any wiring constraints, e.g. to allow operation in the presence of faults.

5.11 Controller Noise

The total system noise shall be limited by the device noise performance with a single double correlated sampling readout mode. The typical read noise of the detectors is ~ $15e^-$ (rms).

5.12 Integration Time

The system shall allow integration times ranging from 0 seconds up to 1 hour. (Note: the minimum exposure time used shall be determined by the detector readout mode and window size).

5.13 Over-Voltage Protection

ESO shall give advice to ATC and RAL on how to provide over-voltage protection on the bias voltages, clock voltages and the control signals that are applied to detectors. It is expected that this over-voltage protection will be implemented on the fan-out boards and flex circuits in the test cryostat and camera cryostat.

5.14 Readout Modes

The system shall provide the following readout modes.

a) Double Correlated Sampling Mode - The detector is reset several times and an initial readout is performed, charge is allowed to integrate for a given exposure and a final readout is performed. The final readout is subtracted from the initial readout pixel-by-pixel to obtain a single exposure.

b) Read-Reset-Read Mode - Each row in the detector is read then reset and read again on a line-by-line basis. After the desired integration, the read, reset and read process is repeated on a line-by-line basis. This process will be continued for the desired number of readout frames.

5.15 Window Readout

The system shall be able to acquire and store data from a user-defined region of interest (ROI). It shall be possible to acquire and store data from an ROI on one detector and preferably from identical ROIs on at least two detectors. The ROI on each detector shall be at least 64x64 pixels with a frame rate of at least 10 Hz and preferably 20 Hz.

The definition of ROI may be limited or restricted by the detector architecture. Since each detector is read out simultaneously from all 16 outputs, the ROI can be a strip across the detector with variable number of rows as ROI height. Also, since all the detectors are clocked together, it is advantageous to read the corresponding ROIs from all or at least two detectors across the focal plane to test image motions or tracking errors.

5.16 Detector Control Software

The system shall include Detector Control Software (DCS) as defined in AD05. This software may include components that run both on IRACE hardware and on the Instrument Workstation.

5.16.1 Low Level Control

The software shall allow programming of the controller for various modes of readout, setting bias and clock levels, changing the clock sequence, optimising the signal sampling etc. to allow tuning the detectors for desired performance.

5.16.2 High Level Control

a) The system shall provide a graphical user interface for engineering control and status verification.
b) The system shall allow exposure time, readout mode and number of exposures in a sequence to be defined. The exposure duration shall be definable as a real number, which includes fractions of a second.
c) The system shall provide a command to start an exposure series.
d) Once started, the system shall allow an exposure series to be aborted on demand.
e) The software shall conform to all the ESO requirements stated in AD05 and shall support the standard ESO command interface described in AD08 and implemented in AD09 (and is therefore controllable from ESO Compliant Observation Software).
f) The system shall have the ability to keep a log of the detector status (including clock and bias voltages) and to log errors, alarms and significant events.
g) The system shall provide a status flag indicating when the detectors are being read out.

5.17 Sustained Operation

It shall be possible to perform data acquisition at a sustained rate of one exposure every 10s over a period of 14 hours, assuming there is sufficient data storage space and no reconfiguration is required. This implies a network that is capable of delivering a sustained bandwith of 102.4Mbit/s between the controllers and the number crunching computers. Since a typical network switch begins to exhibit substantial packet loss above ~15% sustained utilisation, this will require a specified network bandwidth in excess of 670Mbit/s to realise this mode of operation.

5.18 Grounds and EMI Shields

It is important to have all ground connections under control to allow connection to a 'star' ground point of the entire camera system in order to achieve the best noise performance. An appropriate grounding and signal-shielding scheme among the distributed controller units shall be provided. Each controller unit shall also have EMI shielding in order to prevent the interference with the other controller units.

These procedures shall comply with the general design requirements specified in AD02 and with the EMC requirements given in AD03 and AD04 and be tested in accordance with AD06.

5.19 Controller Drift

The drift in the controller output voltages that are applied to detectors should be less than 200 ppm/K (TBC).

5.20 Gain Stability

The gain stability / drift of the video processing chain shall be less than 200 ppm/K (TBC).

5.21 Data Storage

a) It shall be possible to store data in any of the following forms:
- Raw data
- Raw data after differencing
- Co-added differenced data
- Co-added read-reset-read sequence

Any set of data shall be stored in one form only.

b) All data shall be stored as signed 32 bit integers.

c) The raw data shall be stored in a FITS format conforming to the ESO Data Interface Control Document [AD10].

d) The system shall deliver the raw data in a consistent and predictable pixel order. It shall possible, with appropriate calibration of detector connectivity, to determine from which detector and pixel any data element originates.

e) Raw data shall be stored with sufficient metadata to describe accurately each exposure. Metadata shall include as a minimum:
- The detector controller identity and status
- The identity and location of each chip
- A time stamp of the exposure and the readout clock pattern
- The exposure duration

5.22 Controller Cross-talk

The cross-talk shall be limited by the device cross-talk performance. Typical cross-talk between readouts in the detector is expected to be < 0.01%.

5.23 Dynamic Range

The system shall support the dynamic range that the detectors possess. It shall be possible to select a system gain that is well matched to the charge handling capacity of the detectors while the system noise is being sampled adequately.

5.24 Non-linearity

The controller non-linearity shall be less than 0.1% over the full dynamic range specified under simulated test conditions. i.e. if a DC input voltage is applied in steps to a video processing chain, the digitised data shall be proportional to the input and the non-linearity shall be less than 0.1% (peak to valley).

5.25 Controller Power Supply

Each electronics unit shall include its own integral power supply satisfying all the low voltage and power requirements. The power supply shall accept an input of 220-240VAC, 50-60Hz.

5.26 Exchangeability

The DFE units shall be readily interchangeable with each other with any detector dependent parameters being settable under software control. Similarly any other electronics shall be exchangeable with another (spare) electronics unit produced to the same specification.

5.27 ESO Compliance

The system shall be ESO compliant with regards to design and implementation including the requirements in AD02 AD03, AD04, AD05, and AD07. If a change to the existing IRACE or any of its modules is proposed by ESO prior to the acceptance of VISTA at Paranal, the change will be adopted at the VPO's sole discretion prior to ESO acceptance at Paranal. If accepted, the changes will be given to the VPO by ESO as Free Issue.

5.28 Controller Power Dissipation and Heat Exchange

Each DFE unit shall include a heat exchange mechanism and temperature controller capable of maintaining the exterior temperature of the DFE thermal enclosure within +1.5K to –5K from ambient temperature in the telescope enclosure.

5.29 Gravity and Earthquake Loadings

The DFEs shall operate under all orientations of 0 - 90 degrees in elevation and 360-degree in cassegrain rotator with respect to gravity. The DFEs and controllers shall comply with the standard ESO environmental specifications with respect to operability following an earthquake. If the amplification of the ground accelerations at the cassegrain focus of VISTA exceed ESO standards (number to be obtained from ESO) then VPO should inform ESO and the issue should be settled either by VISTA compliance with environmental specification, or a waiver (TBC).

5.30 Mechanical

The master & slave DFE units must conform to the following interface :

Parameter	Master DFE	Slave DFE	Notes
Maximum external dimensions, including water cooled enclosure	600 x 575 x 345 mm	600 x 575 x 345 mm	2 Slave DFEs may reside in one water cooled enclosure
Mounting footprint	TBD	TBD	
Maximum weight	40 kg	40 kg	
Connectors	TBD	TBD	
Coolant connections	TBD	TBD	

6 ESO and VPO Responsibilities

The IRACE system is assumed to include the following components:

- Front end electronics
- Back end electronics
- Number Cruncher workstation(s) with GIGA-PCI interface cards performing the DBE functions.
- Cabling between the above
- All software that runs on the above
- Detector Control Software (DCS) and Real Time Display (RTD) software that runs on the Instrument Workstation as described in AD11

The 'Test IRACE' System shall be able to operate standalone i.e. acquire, store and display data from one or two detector arrays. It shall have a 10/100 Mbps Ethernet connection. It shall drive these arrays at the full pixel rate, but need not meet frame rate requirements.

The IRACE System shall operate with the Instrument Workstation, controlling all 16 detector arrays at full performance. Communications between the Number Cruncher workstation(s) and the Instrument Workstation shall use media, protocols and interfaces agreed with ESO. (It is recognised that ESO standards in this area may be updated.)

ESO shall provide:

- Front End Electronics
- Number Cruncher workstation(s) with GIGA-PCI interface cards performing the DBE functions.
- Cabling and mounting hardware
- Instrument Workstation including storage
- All software that runs on the Front and Back End Electronics
- All software that runs on the Number Cruncher workstation(s)
- DCS and RTD software that runs on the Instrument Workstation
- Specification of Instrument Workstation
- Effort to configure and commission a complete IRACE controller system in UK
- Initial guidance on how to use the system

The VPO will provide:

- Network connections between the Instrument Workstation and the Number Cruncher workstation(s)
- Fanout boards to interface DFEs to detectors

7 DOCUMENTATION

The System shall be uniquely identified and supplied with a user manual and technical reference manual both in hard copy and electronic version, which provides:

a) Controller description, boards identification and their location in the controller

b) Operating instructions and IRACE safety procedures

c) Controller software programming instructions

d) Details of low level programming, scripts or language

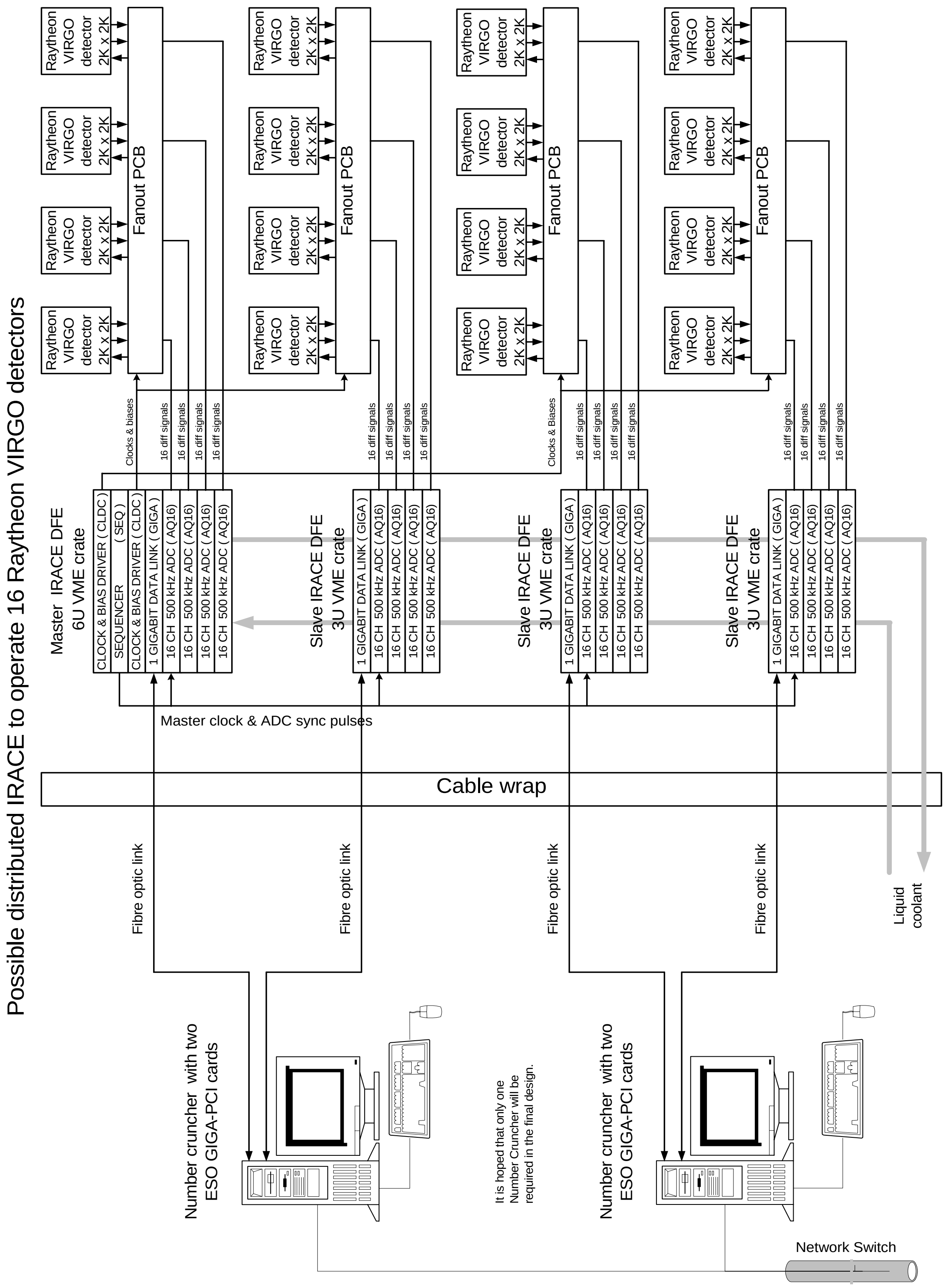
e) Definitions and specifications of user Input Output signals

f) Description of each module and its interface details

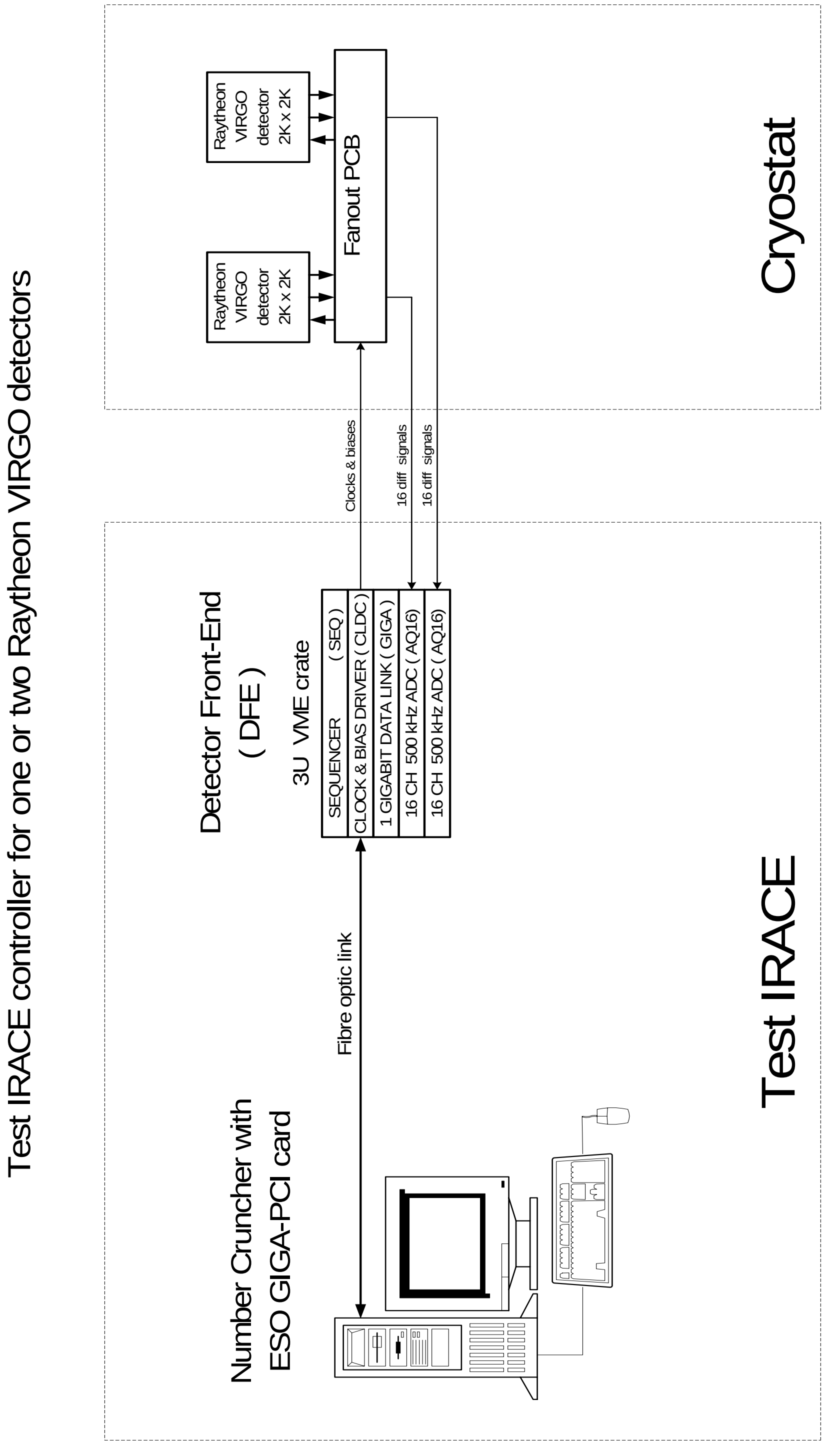
g) A complete drawing set including schematics of electronics, PAL equations and Transputer code.

h) All test data.

Appendix – 1


Possible distributed IRACE to operate 16 Raytheon VIRGO detectors
Raytheon VIRGO detector 2K x 2K
Fanout PCB
Clocks & biases
16 diff signals
Master IRACE DFE 6U VME crate
CLOCK & BIAS DRIVER (CLDC)
SEQUENCER (SEQ)
1 GIGABIT DATA LINK (GIGA)
16 CH 500 kHz ADC (AQ16)
Slave IRACE DFE 3U VME crate
Master clock & ADC sync pulses
Cable wrap
Fibre optic link
Liquid coolant
Number cruncher with two ESO GIGA-PCI cards
It is hoped that only one Number Cruncher will be required in the final design.
Network Switch

Appendix – 2


Test IRACE controller for one or two Raytheon VIRGO detectors
Raytheon VIRGO detector 2K x 2K
Raytheon VIRGO detector 2K x 2K
Fanout PCB
Cryostat
Clocks & biases
16 diff signals
16 diff signals
Detector Front-End (DFE)
3U VME crate
SEQUENCER (SEQ)
CLOCK & BIAS DRIVER (CLDC)
1 GIGABIT DATA LINK (GIGA)
16 CH 500 kHz ADC (AQ16)
16 CH 500 kHz ADC (AQ16)
Fibre optic link
Number Cruncher with ESO GIGA-PCI card
Test IRACE

Appendix - 3

Clock Levels and Bias Voltages required for Raytheon VIRGO Multiplexer

Signal	**Description**	**Level**
Clocks		
PMC	Master Clock for Digital Clocking 200KHz	0 to 4V
FSTART	Start Pulse for New Frame Clocking	0 to 4V
Control Signals		
REDUCEOUT	Control to Select No. of Outputs	0 to 4V
RSTEN	Control to Reset Frame	0 to 4V
RSTSEL	Control to Select Global or Row Reset	0 to 4V
Bias Voltages		
VPUC	Unit Cell Bias	3.5V
VNUC	Unit Cell Return	1.0V
VNOUT	Output Source Follower Return	2.5V
VSUB	Ground Reference	0.0V
VDETCOM	Detector Common	1.0V
VUCRST	Unit Cell Reset Voltage	0.0V
VPD	Digital Bias	4.0V
VND	Digital Return	0.0V
VCAS	Cascode supply for digital	3.0V
VHIRESET	High rail for reset clock	4.0V
VLORESET	Low rail for reset clock	0.0V
VHIROWEN	High rail for row enable	5.0V
VLOROWEN	Low rail for row enable	1.0V
Biases for current sources		
VIDLEREF	Bias for Idle current source (column bus)	-2.35V
VSLEWREF	Bias for Slew current source (column bus)	-3.35V

Outputs

16 outputs at up to 400 kHz pixel rate

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